Electronic Version
Stylesheet Version v1.1.1

A Muxed-Output Double-Date-Rate-2 (DDR2) Register with Fast Propagation Delay

Abstract

A register chip for double-data-rate (DDR) memory modules operates in 1:1 mode or 1:2 mode. A differential input clock is buffered to generate a slave clock that continuously clocks slave stages of flip-flops, and gated to generate a first clock pulsing only in 1:1 mode and a second clock pulsing only in 1:2 mode. The master stage has two input transmission gates, one activated by the first clock and another activated by the second clock. In 1:1 mode a first data bit is sampled by the first clock, but in 1:2 mode a second data bit is sampled by the second clock. The sampled bit is inverted and applied to the slave stage and to a feedback gate that has transistors gated by the first and second clocks. The clock-to-output delay is improved since an output mux is replaced by the muxing function built into the master stage.